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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,721	06/25/2003	Chandra Mouli	M4065.0761/P761	9931

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EXAMINER	
LEE, EUGENE	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,721	MOULI ET AL.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-58* is/are pending in the application.

4a) Of the above claim(s) *38-58* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/26/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I (1-37) in the reply filed on 8/31/04 is acknowledged.

2. Claims 38 thru 58 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 8/31/04.

Specification

3. The disclosure is objected to because of the following informalities: on page 4, paragraph [0013], line 3, there is a word missing in between the phrases "where the " and "and photodiode".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 thru 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koizumi et al. 6,661,459 B1 in view of Kimata 4,760,273. Koizumi discloses (see, for example, FIG. 3) a pixel cell comprising a p-well (substrate) 102, transfer gate region (gate) 103, transfer transistor,

and a photoelectric conversion element wherein the photoelectric conversion element comprises a p-layer (doped surface layer of a first conductivity type) 105, and n-layer (doped region of a second conductivity type) 106. Koizumi does not disclose a gate of a transistor formed at least partially below the surface of the substrate. However, Kimata discloses (see, for example, FIG. 5) a transfer transistor comprising a transfer gate electrode 14 in a groove (below the surface of the substrate) 8a. In column 6, lines 21-25, Kimata discloses that forming the transfer gate electrode in the groove decreases the area occupied by the transfer gate electrode on the main surface of the semiconductor substrate. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a gate of a transistor formed at least partially below the surface of the substrate in order to decrease the area occupied by the transfer gate electrode on the main surface of the semiconductor substrate.

Regarding claim 3, see FIG. 3 wherein Koizumi discloses a p-layer 105 and n-layer 104 which collectively form a pinned photodiode.

Regarding claim 4, see column 4, line 19 wherein Koizumi discloses a transfer transistor.

Regarding claims 5, 6, 18, and 19, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed (i.e. in a reset transistor or charge coupled device) does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations, Ex Parte Masham, 2 USPQ F. 2d 1647 (1987).

Regarding claims 7 and 8, see FIG. 3 wherein Koizumi discloses a floating diffusion (sensing node) 107.

Regarding claim 9, Koizumi in view of Kimata does not disclose the doped surface layer having a thickness within the range of approximately 200 to approximately 2000 A. However,

the thickness of the doped surface layer is a result effective variable that one of ordinary skill in the art would optimize for forming the photodiode in a semiconductor device. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have the doped surface layer have a thickness within the range of approximately 200 to approximately 2000 A, in order to form an adequate photodiode in a semiconductor device, and since it has been held that discovering the optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 10, the implant dose is a product-by-process limitation of forming the doped surface layer. Such a process limitation does not impart any structural limitations to the final product.

Regarding claims 13 and 21, Koizumi in view of Kimata does not disclose the trench having a depth within the range of approximately 500 to approximately 2500 A. However, the depth of the trench is a result effective variable that one of ordinary skill in the art would optimize for forming the transfer gate in a semiconductor device. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have the trench have a depth within the range of approximately 500 to approximately 2500 A in order to form an adequate gate in a semiconductor device, and since it has been held that discovering the optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claims 14 and 22, see FIG. 5 wherein Kimata discloses an insulating film (insulating material) 10.

Regarding claims 15, 16, and 23, Koizumi in view of Kimata does not disclose the insulating material on the two lateral sides of the gate has a thickness within the range of approximately 20 to approximately 100 A thick. However, the thickness of the insulating material is a result effective variable that one of ordinary skill in the art would optimize for affecting the operation of a transfer gate in a semiconductor device. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have the insulating material on the two lateral sides of the gate has a thickness within the range of approximately 20 to approximately 100 A thick in order to form an adequate gate insulating material around the gate electrode, and since it has been held that discovering the optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980).

6. Claims 24 thru 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koizumi et al. '459 B1 in view of Kimata '273 as applied to claims 1-23 above, and further in view of Furumiya et al. 6,639,293 B2. Koizumi in view of Kimata does not disclose a processor. However, Furumiya discloses (see, for example FIG. 1) an analog signal processor 6 coupled to an imaging unit (imager) 2. In column 1, lines 2-5, Furumiya discloses the analog signal processor as amplifying and processing signals from selected pixels. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a processor in order to amplify and process signal from the pixels.

Regarding claims 25 and 26, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed (i.e. in a CMOS imager or charge

coupled device imager) does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations, Ex Parte Masham, 2 USPQ F. 2d 1647 (1987).

Regarding claim 28, see FIG. 3 wherein Koizumi discloses a p-layer 105 and n-layer 104 which collectively form a pinned photodiode.

Regarding claims 31 and 32, see FIG. 3 wherein Koizumi discloses a floating diffusion (sensing node) 107.

Regarding claim 33, Koizumi in view of Kimata in view of Furumiya does not disclose the doped surface layer having a thickness within the range of approximately 200 to approximately 2000 A. However, the thickness of the doped surface layer is a result effective variable that one of ordinary skill in the art would optimize for forming the photodiode in a semiconductor device. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have the doped surface layer have a thickness within the range of approximately 200 to approximately 2000 A, in order to form an adequate photodiode in a semiconductor device, and since it has been held that discovering the optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 36, Koizumi in view of Kimata in view of Furumiya does not disclose the trench having a depth within the range of approximately 500 to approximately 2500 A. However, the depth of the trench is a result effective variable that one of ordinary skill in the art would optimize for affecting the transfer gate in a semiconductor device. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have the trench having a depth within the range of approximately 500 to approximately 2500 A in

order to form an adequate gate in a semiconductor device, and since it has been held that discovering the optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980).

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee
September 14, 2004